



PATENT ABSTRACTS OF JAPAN

(11) Publication number: **07093972 A**(43) Date of publication of application: **07.04.95**

(51) Int. Cl.

G11C 11/407
G11C 11/409
(21) Application number: **05239297**(71) Applicant: **SONY CORP**(22) Date of filing: **27.09.93**(72) Inventor: **HASHIGUCHI AKIHIKO**(54) **SEMICONDUCTOR MEMORY DEVICE**

(57) Abstract:

PURPOSE: To realize a high-speed semiconductor memory device which can generate the activation timing of a sense amplifier without being affected by an irregularity in a process.

CONSTITUTION: When one word line is activated, a voltage VDBL for a dummy bit line DBL which is held at a prescribed potential and a preset reference voltage VBS are compared by a differential-type comparator MCA. When the voltage VDBL becomes the reference voltage VBS or higher, an activation signal SACT is generated, the signal is input to a driver for a sense amplifier S/A, and the sense amplifier is activated.

COPYRIGHT: (C)1995,JPO

